

Fig. 1A

FORMING STEP OF SILICON NITRIDE OXIDE FILM (SiN_xByO_z) 103a BY SPUTTERING

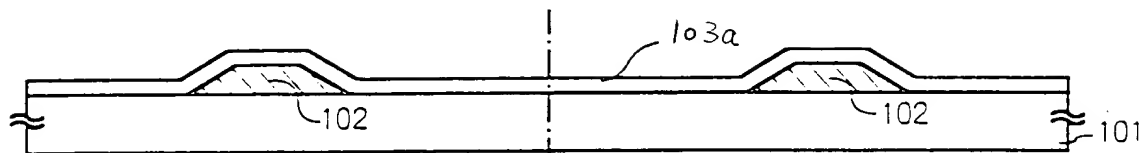


Fig. 1B

FORMING STEP OF INSULATING FILM 103b AND SEMICONDUCTOR FILM

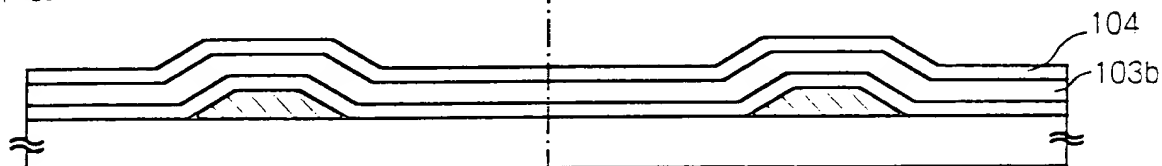


Fig. 1C

LASER CRYSTALLIZATION STEP

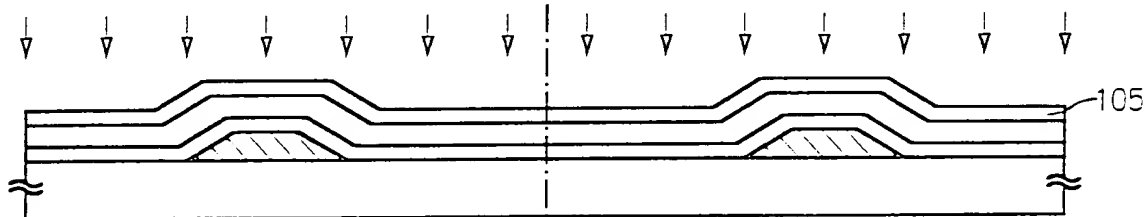


Fig. 1D

BACK EXPOSURE STEP

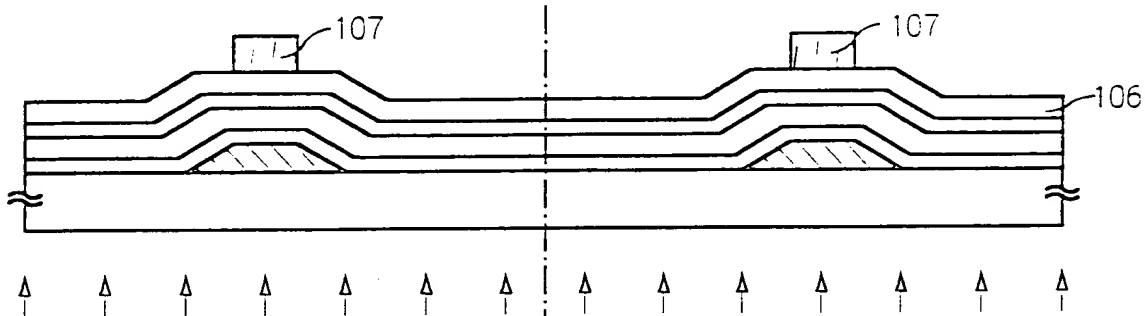
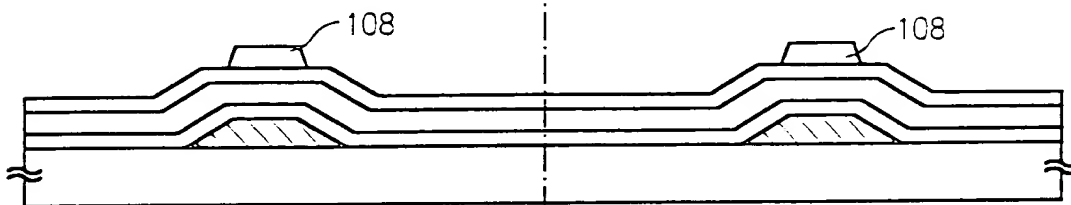


Fig. 1E

ETCHING STEP



N-CHANNEL TFT

P-CHANNEL TFT

Fig. 2A DOPING STEP (FORMING STEP OF n^+ REGION)

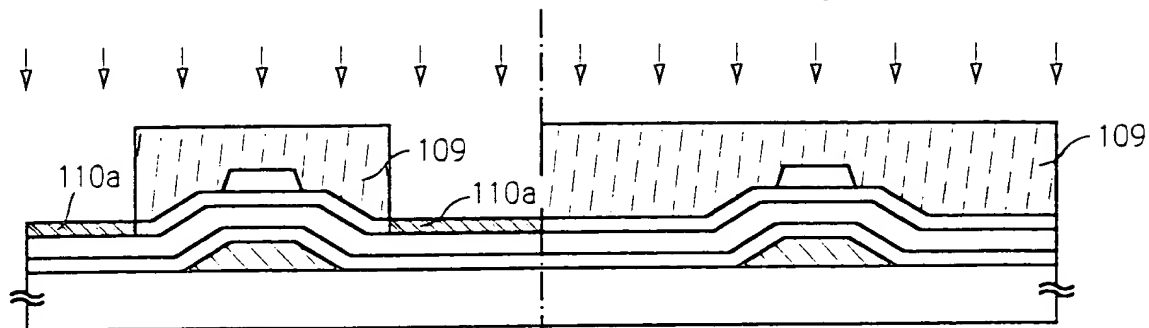


Fig. 2B FORMING STEP OF INSULATING FILM 111

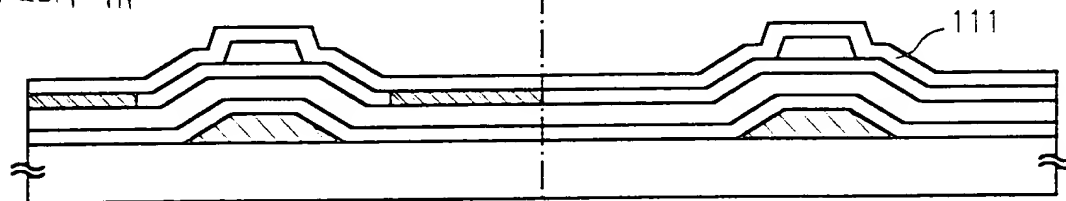


Fig. 2C DOPING STEP (FORMING STEP OF n^- REGION)

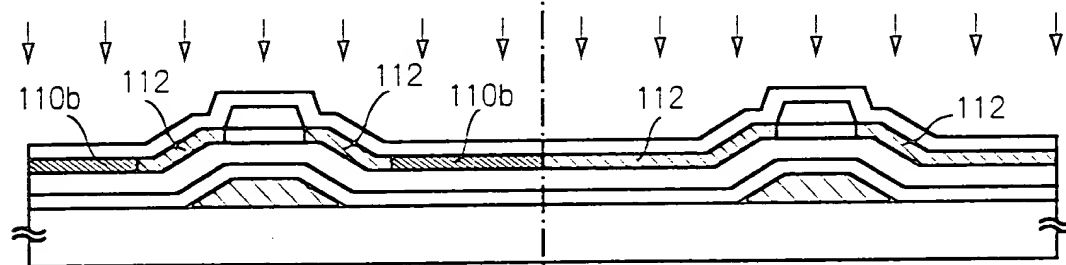
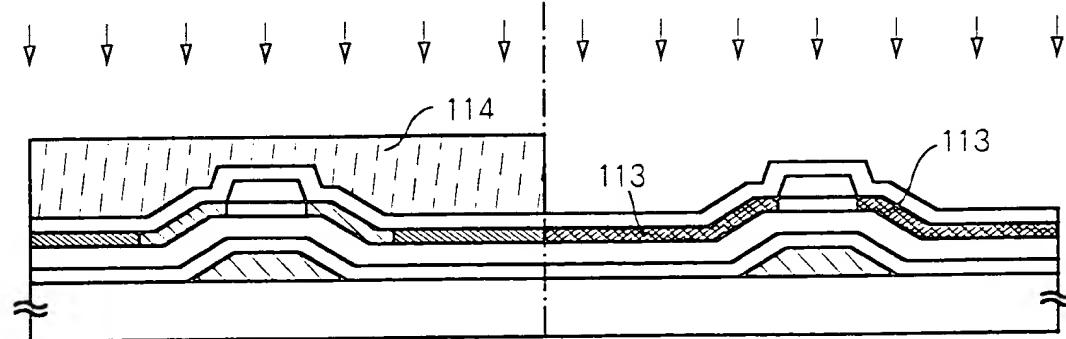


Fig. 2D DOPING STEP (FORMING STEP OF p^+ REGION)



N-CHANNEL TYPE TFT

P-CHANNEL TYPE TFT

Fig.3A ACTIVATION STEP

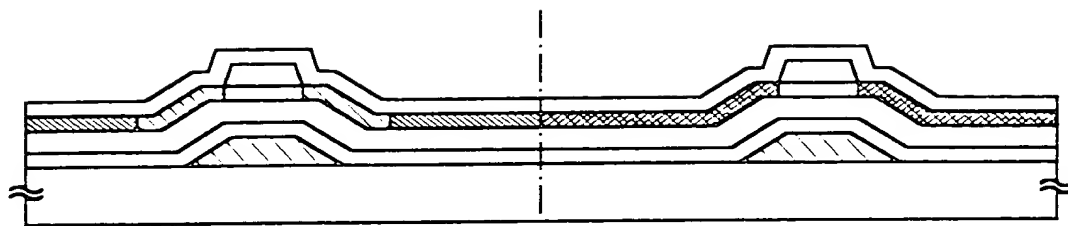


Fig.3B PATTERNING STEP

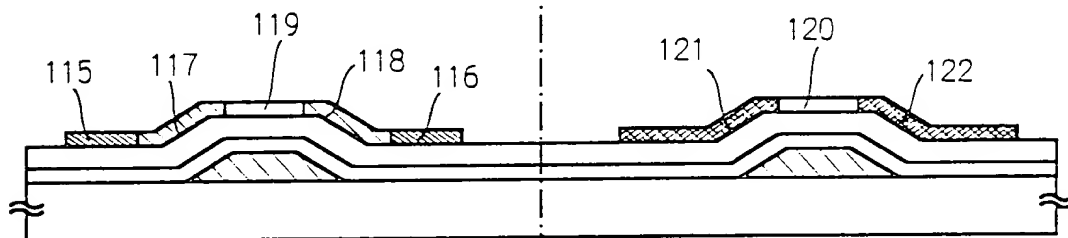


Fig.3C FORMING STEP OF INTERLAYER INSULATING FILM

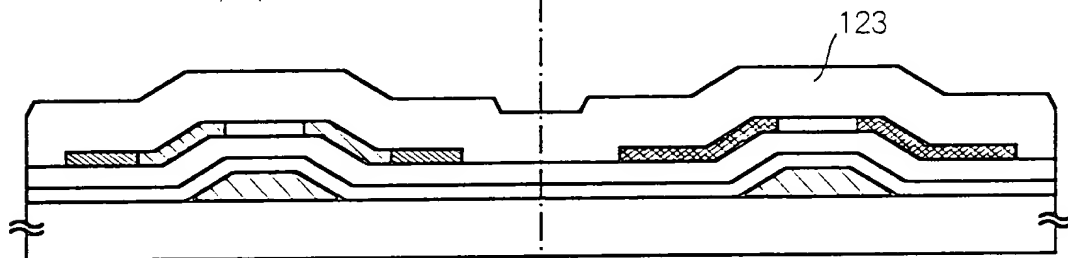
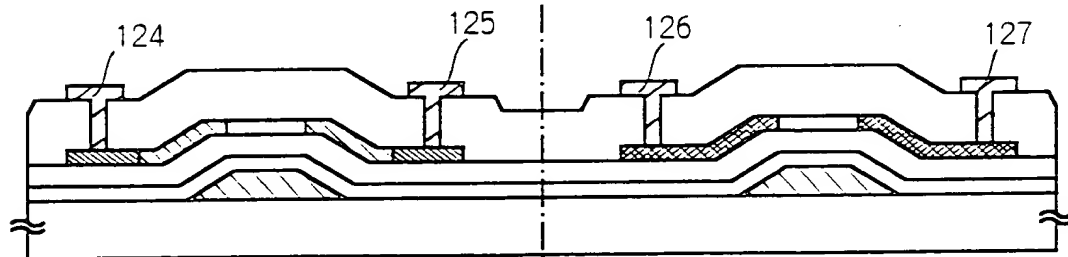


Fig.3D FORMING STEP OF SOURCE WIRING LINE AND DRAIN WIRING LINE



N-CHANNEL TYPE TFT

P-CHANNEL TYPE TFT

Fig.4A

FORMING STEP OF SILICON NITRIDE OXIDE FILM ($\text{SiN}_x\text{B}_y\text{O}_z$) 103a BY SPUTTERING

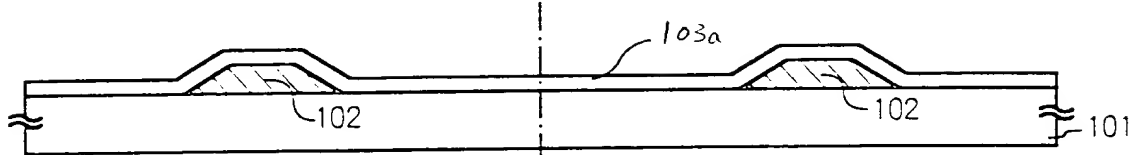


Fig.4B

FORMING STEP OF INSULATING FILM 103b AND SEMICONDUCTOR FILM

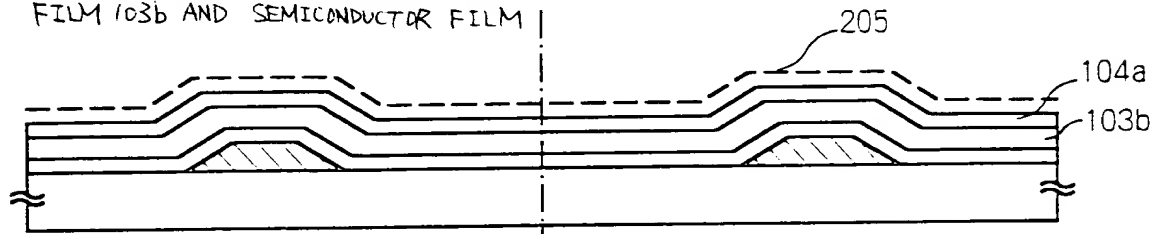


Fig.4C

CRYSTALLIZING STEP BY HEAT TREATMENT

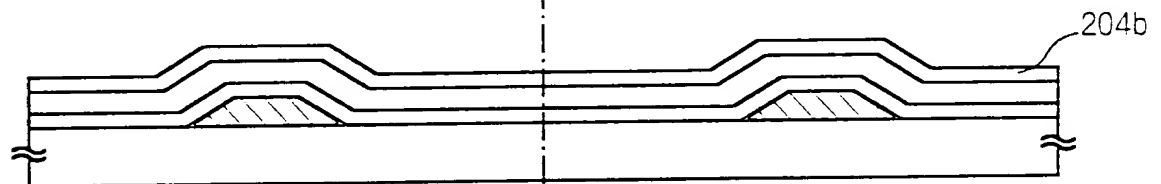


Fig.4D

LASER IRRADIATION STEP

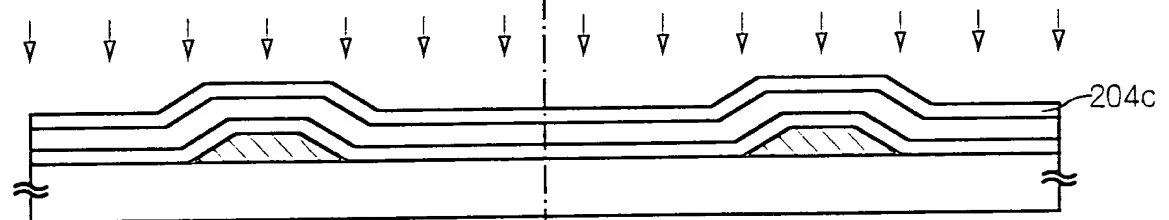


Fig.4E

BACK EXPOSURE STEP

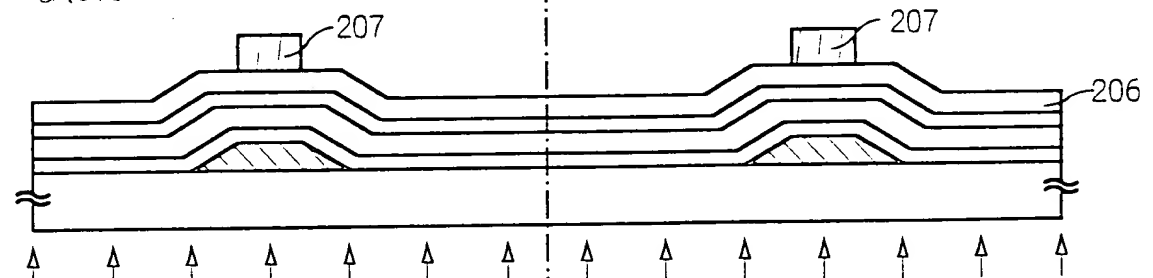


Fig.4F

ETCHING STEP

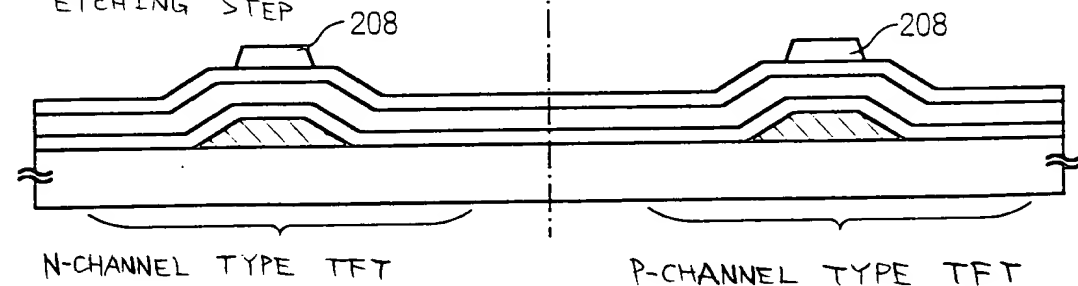


Fig.5A DOPING STEP (FORMING STEP OF n^+ REGION)

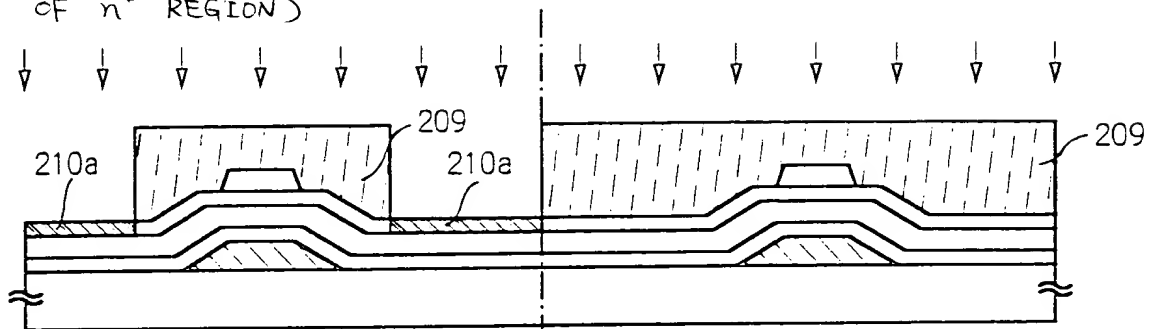


Fig.5B FORMING STEP OF INSULATING FILM 211

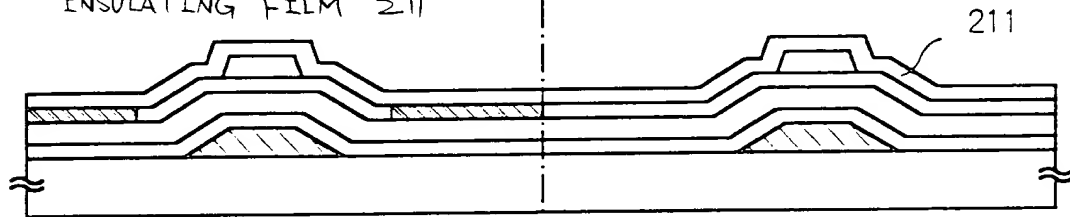


Fig.5c DOPING STEP (FORMING STEP OF n^- REGION)

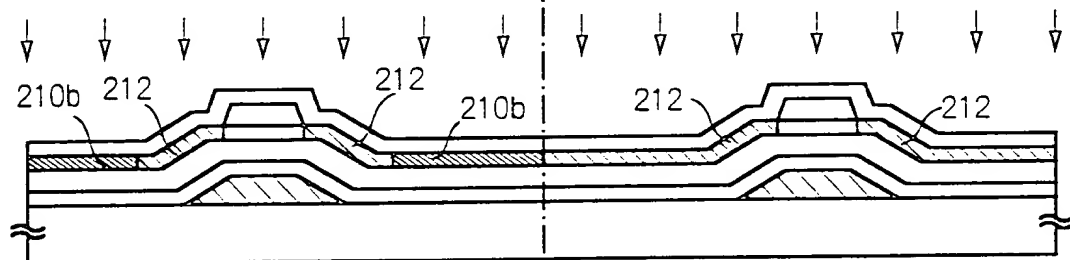
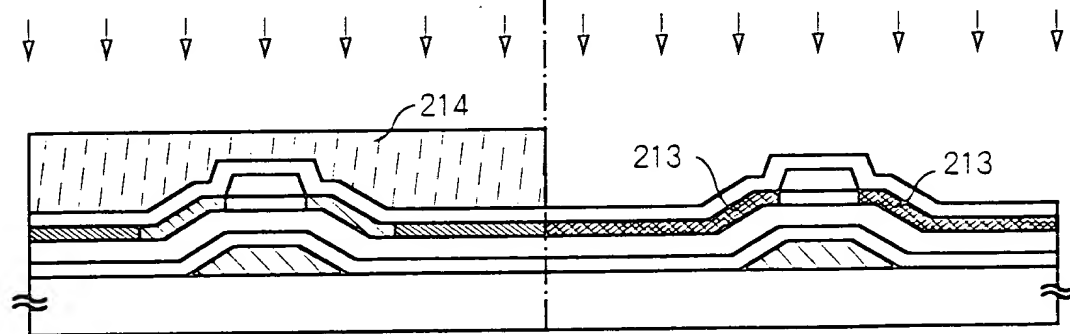


Fig.5D DOPING STEP (FORMING STEP OF p^+ REGION)



N-CHANNEL TFT

P-CHANNEL TFT

Fig. 6A ACTIVATION AND
GETTERING STEP

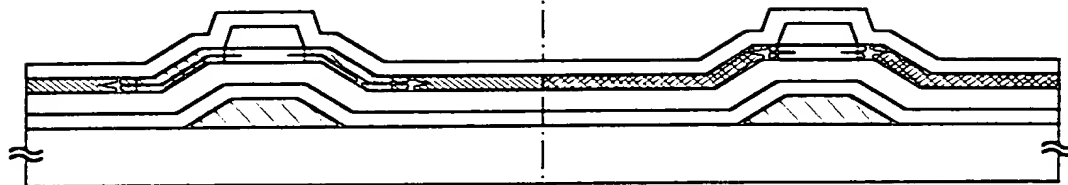


Fig. 6B PATTERNING STEP

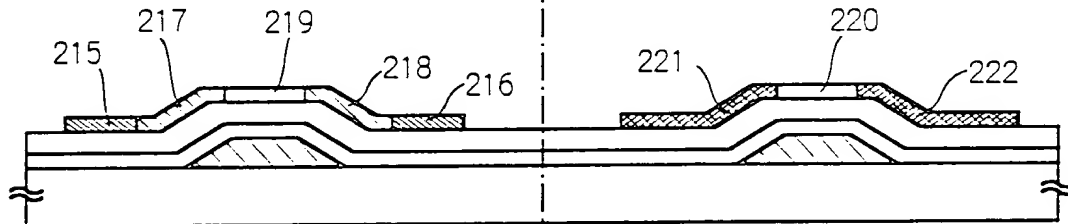


Fig. 6C FORMING STEP OF
INTERLAYER INSULATING FILM

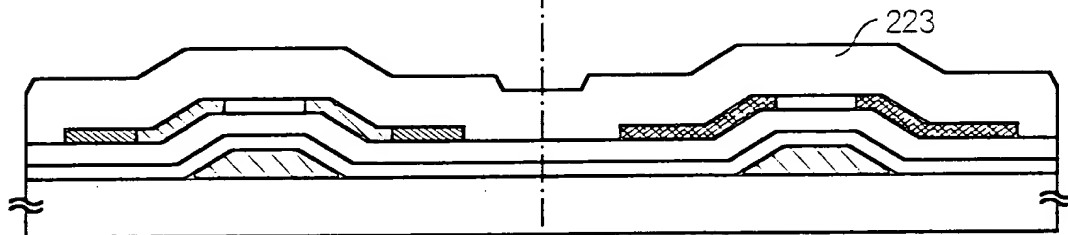
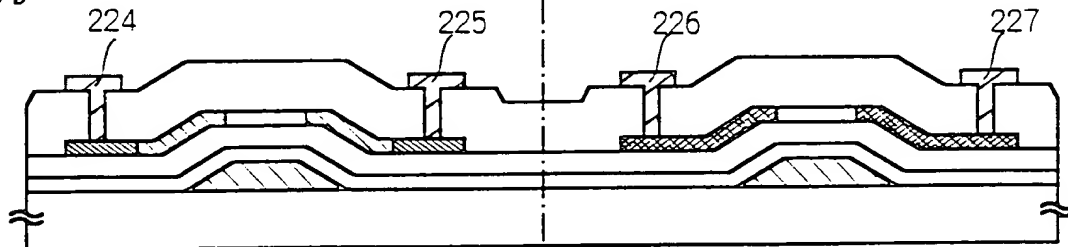


Fig. 6D FORMING STEP OF SOURCE
WIRING LINE AND DRAIN
WIRING LINE



N-CHANNEL TYPE TFT

P-CHANNEL TYPE TFT

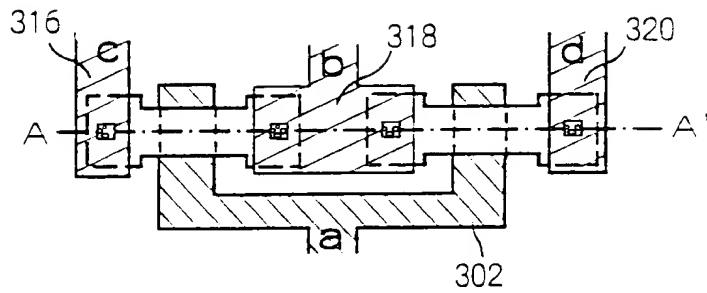


Fig. 7A TOP VIEW OF CMOS CIRCUIT

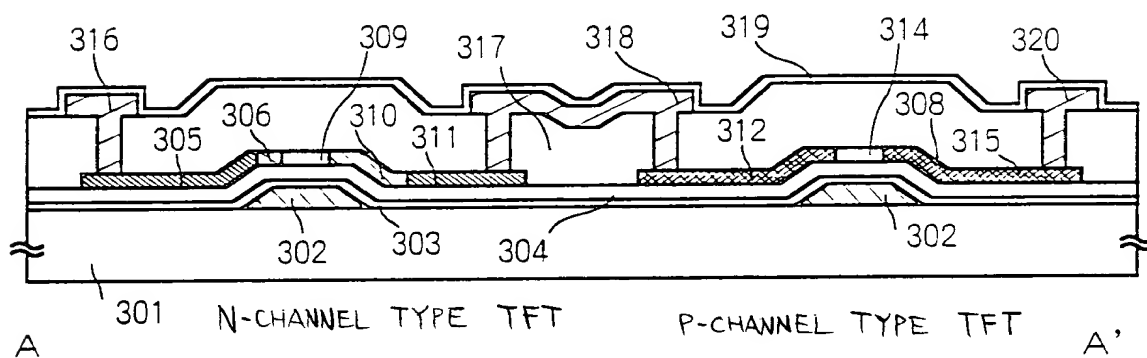


Fig. 7B SECTIONAL STRUCTURE VIEW ALONG A-A'

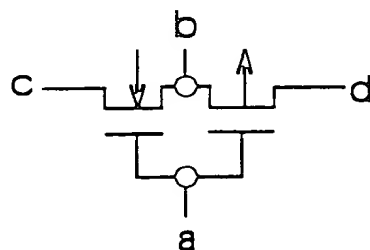


Fig. 7C CIRCUIT DIAGRAM OF CMOS

Fig. 8A TOP VIEW

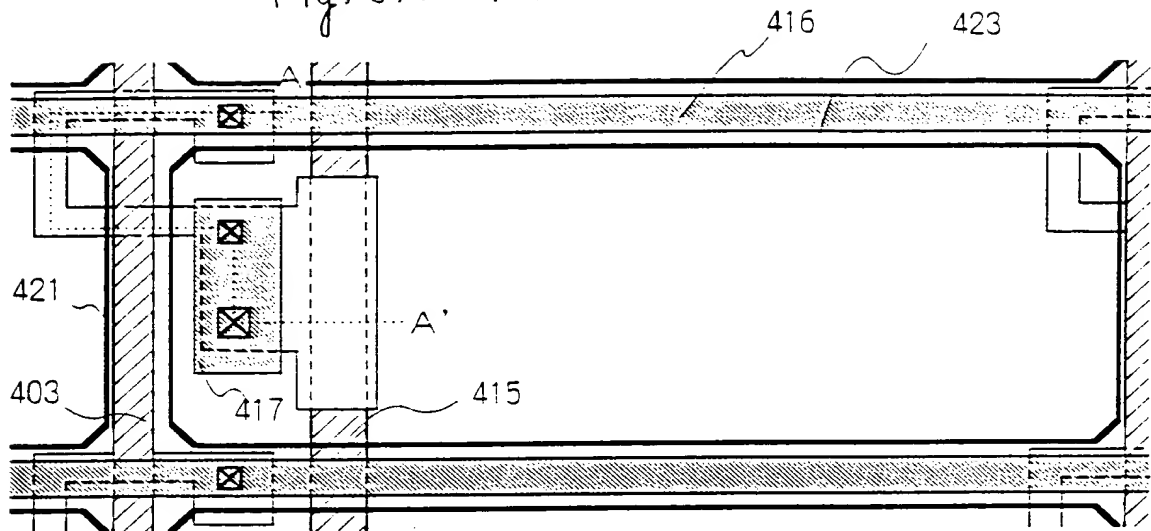
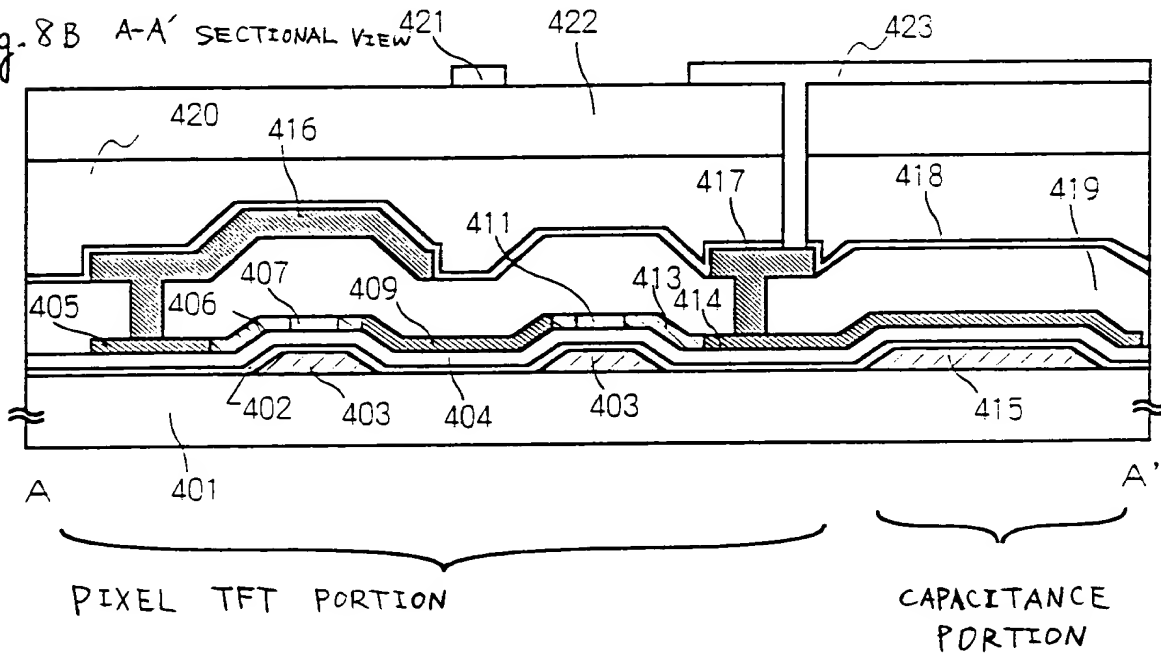
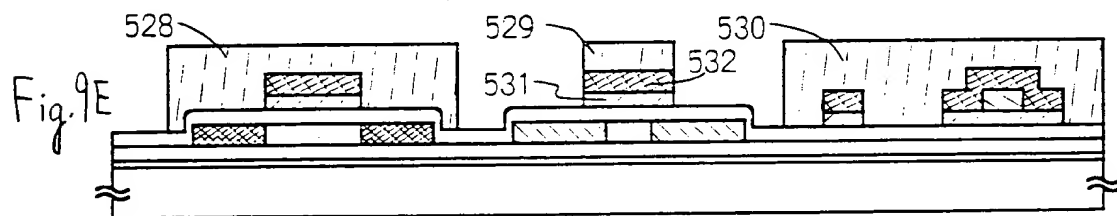
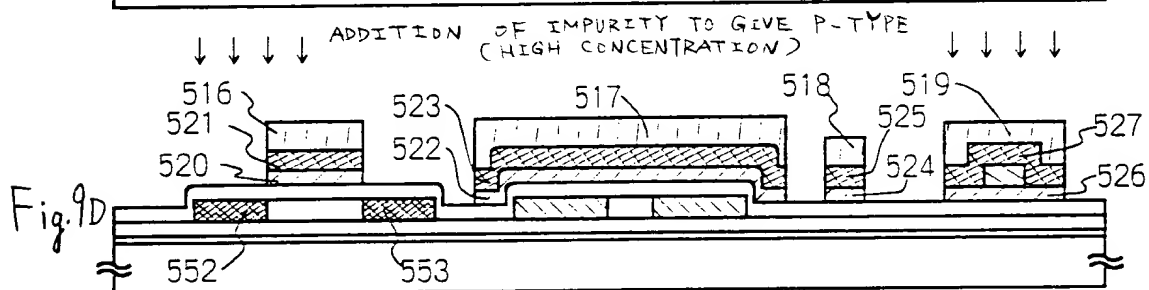
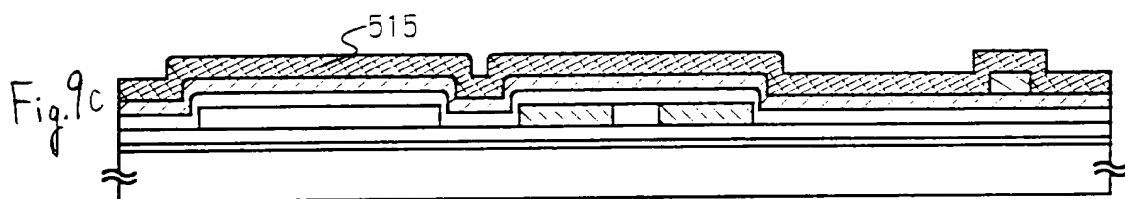
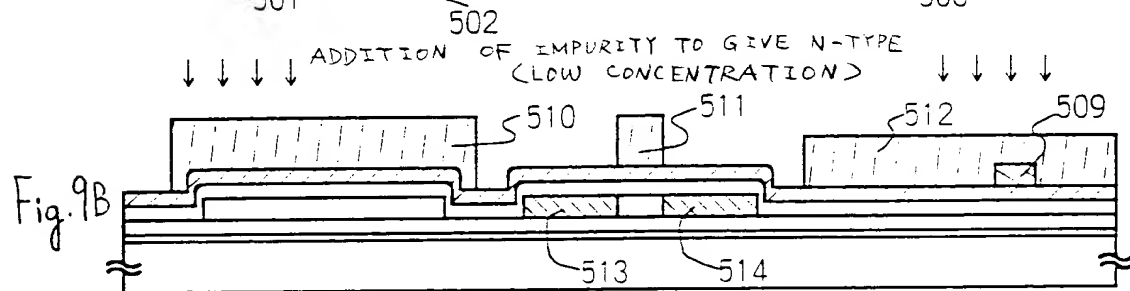
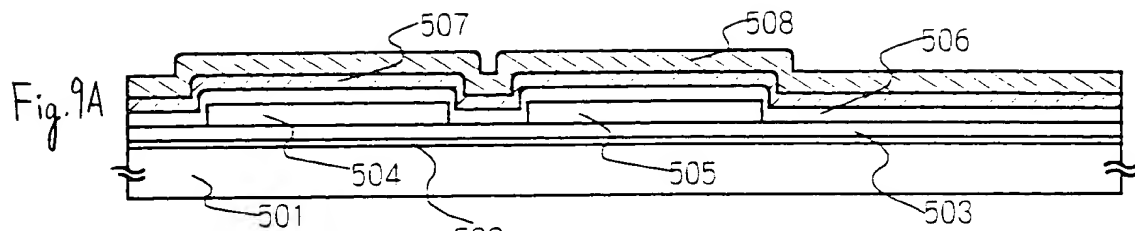


Fig. 8B A-A' SECTIONAL VIEW





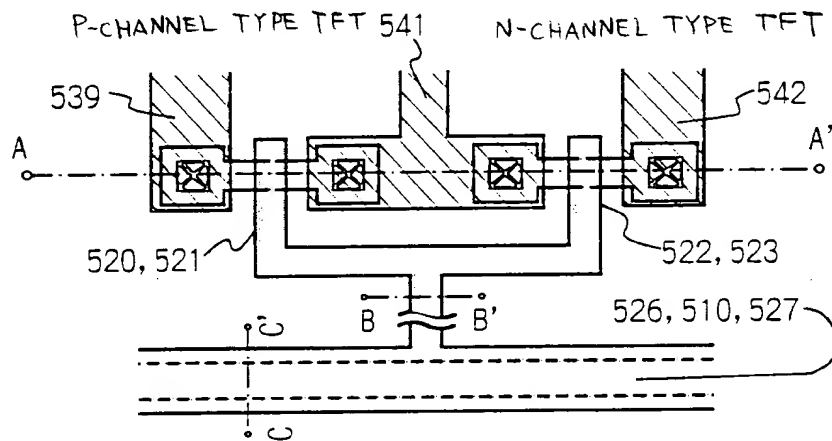
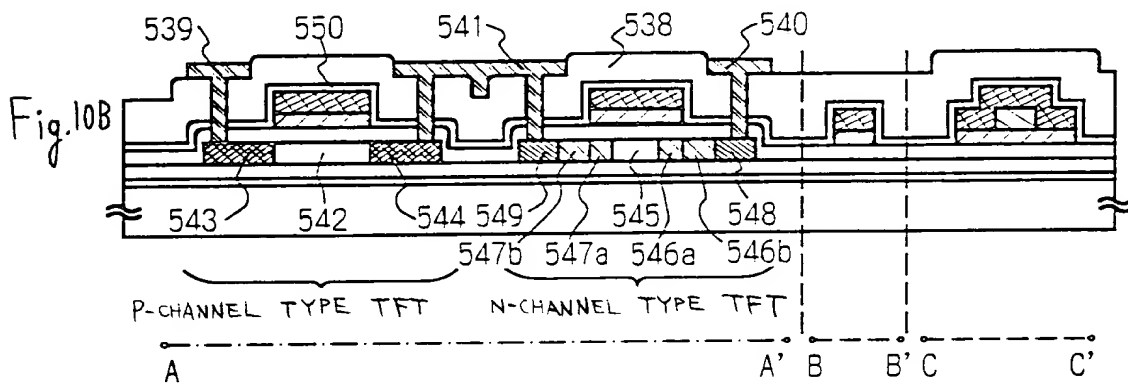
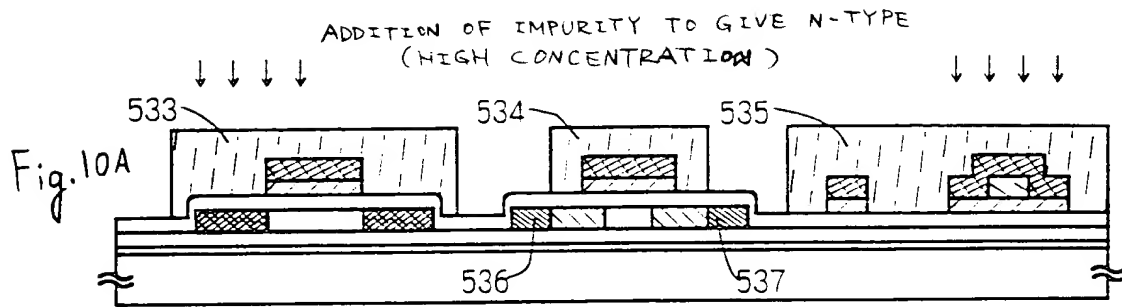
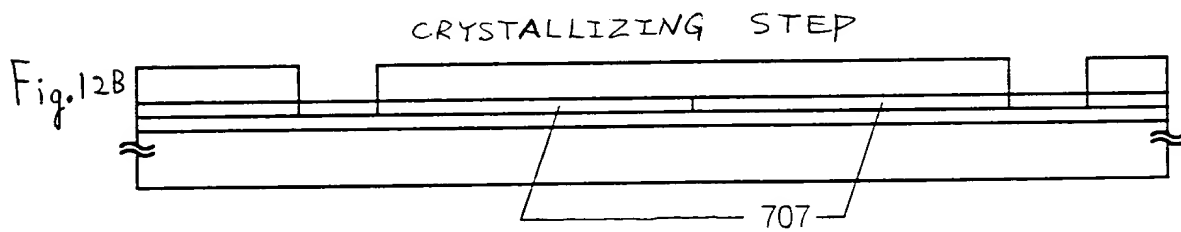
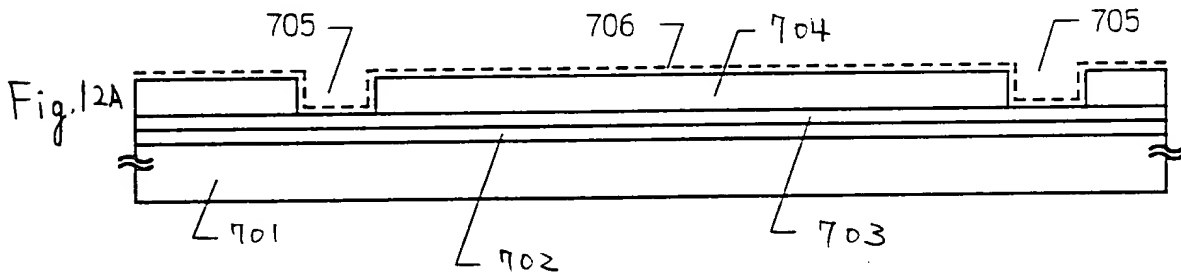
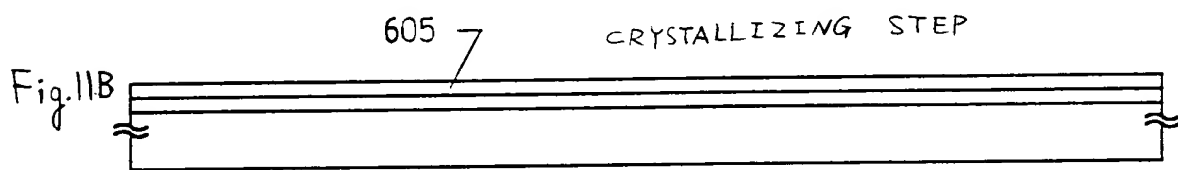
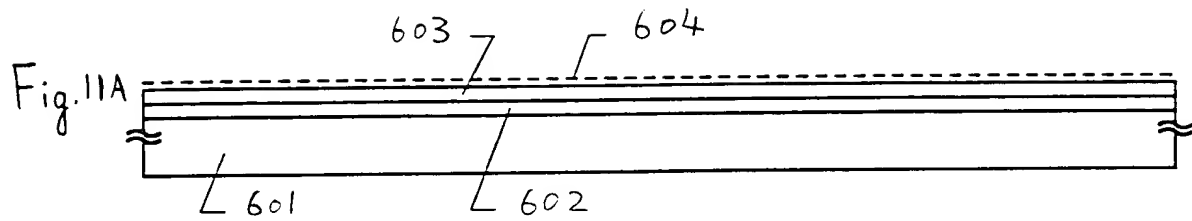


Fig. 10C TOP VIEW OF CMOS CIRCUIT



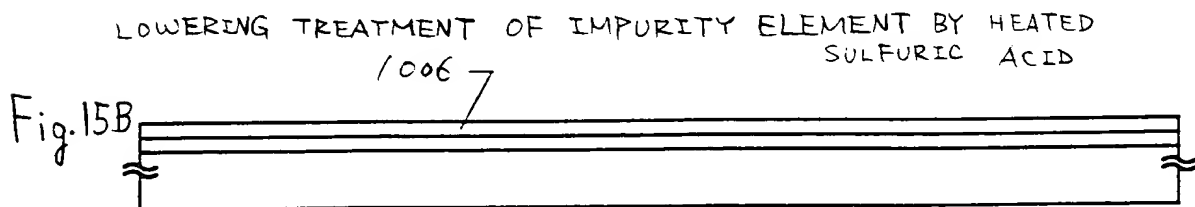
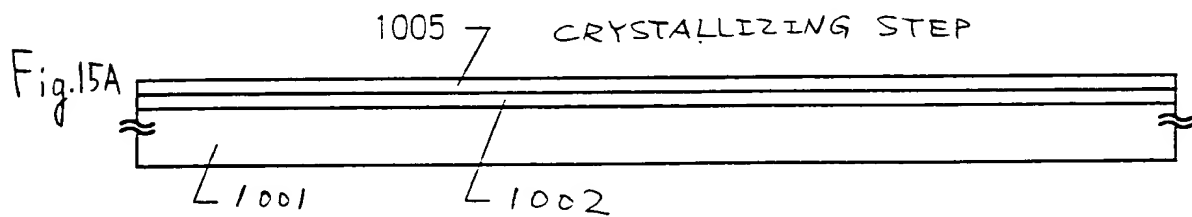
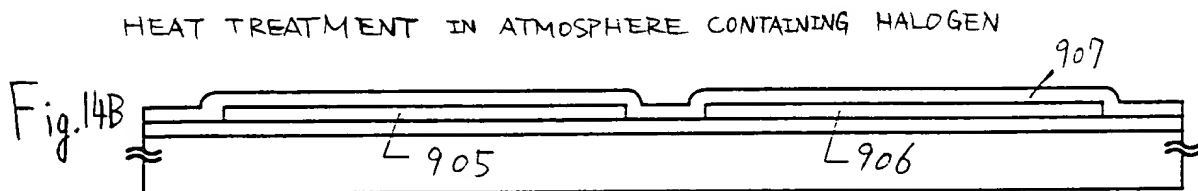
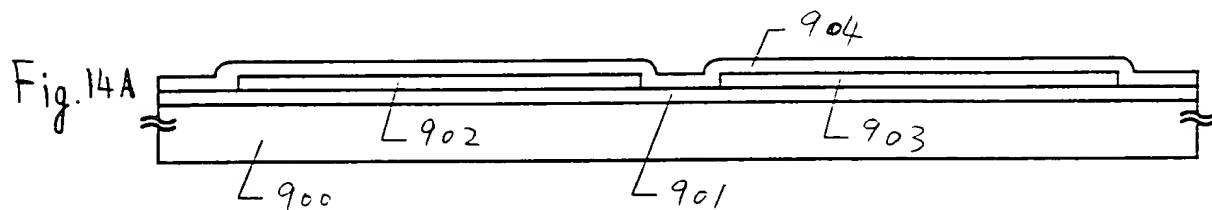
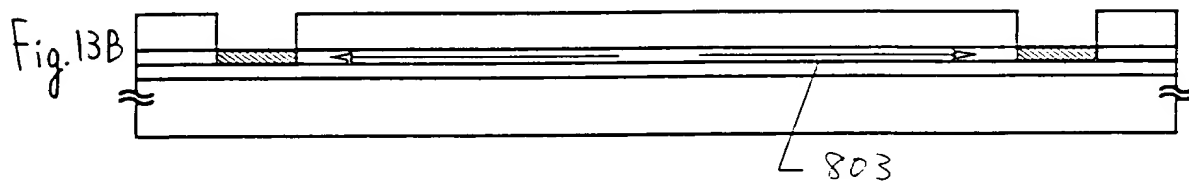
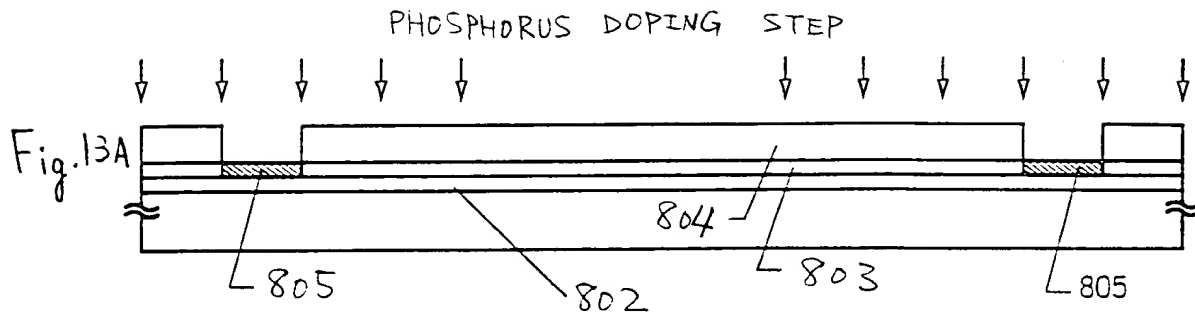


Fig. 16A REVERSE STAGGER TYPE TFT

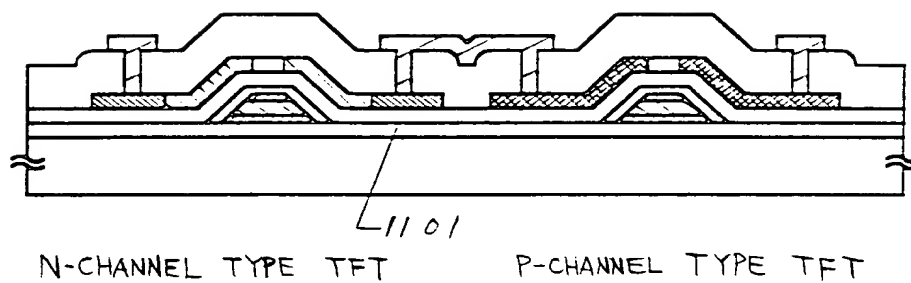


Fig. 16B FORWARD STAGGER TYPE TFT

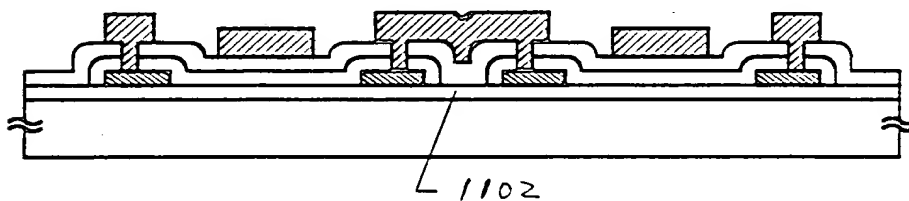
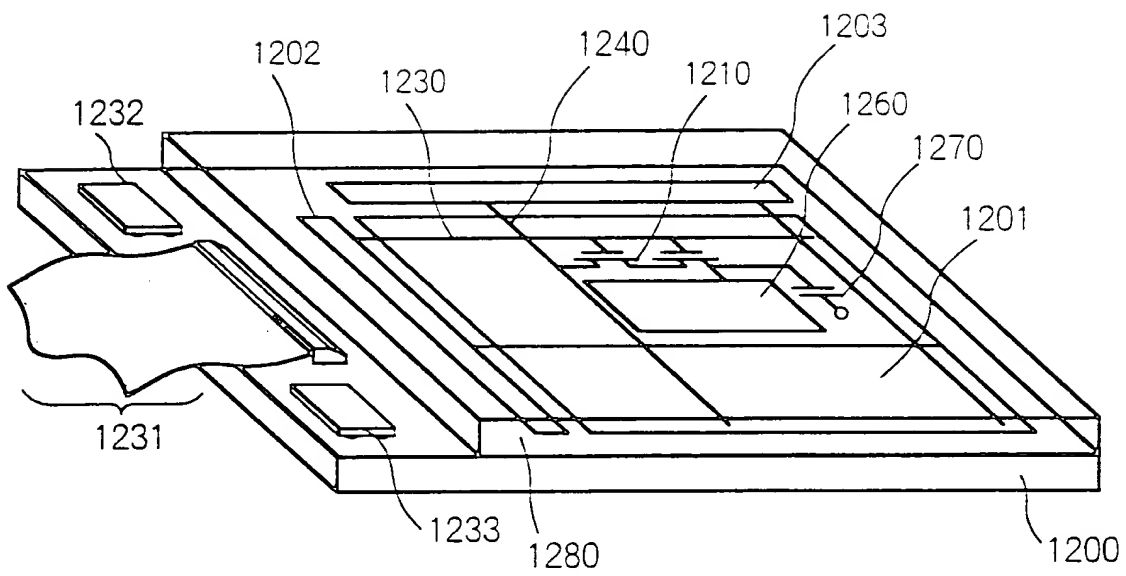
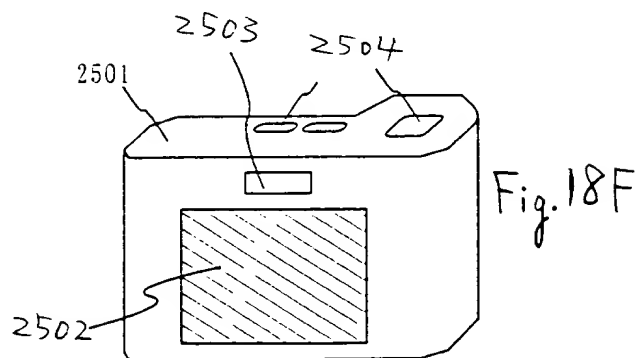
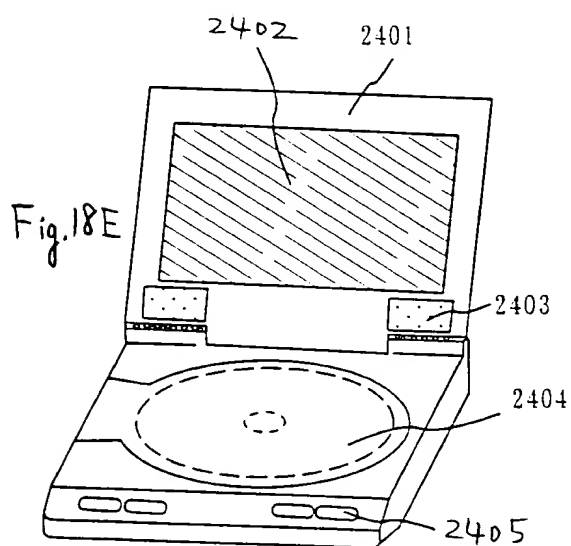
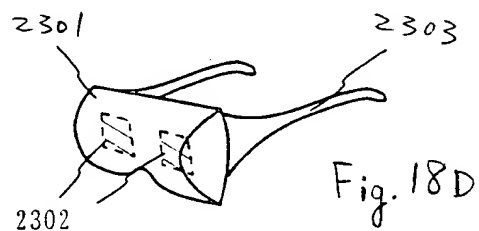
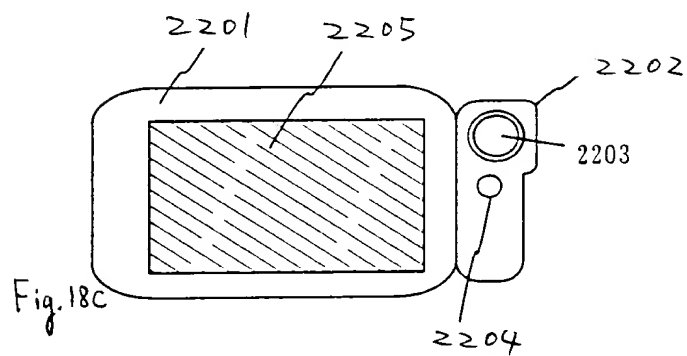
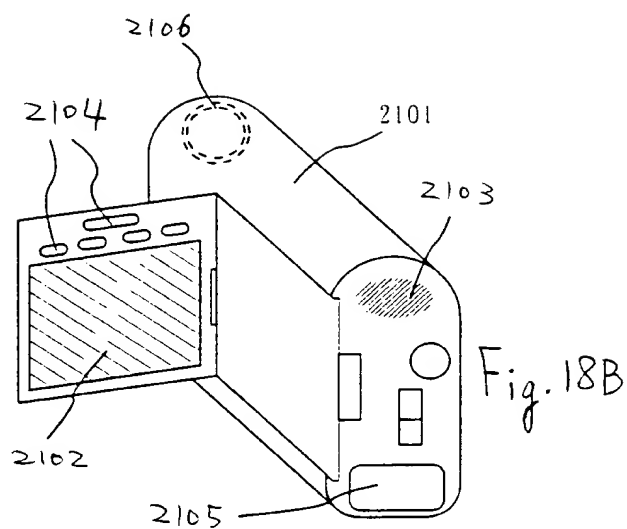
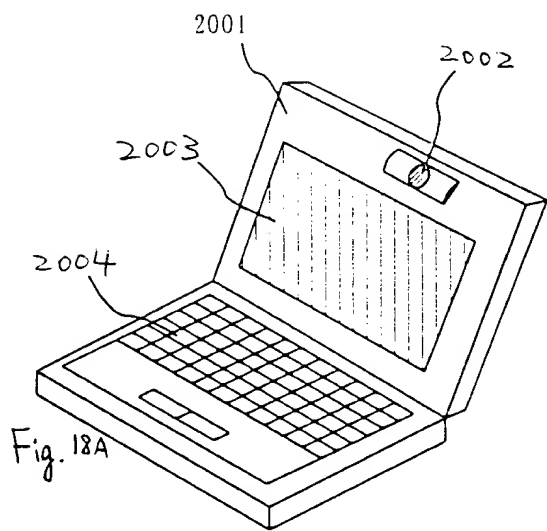


Fig. 17





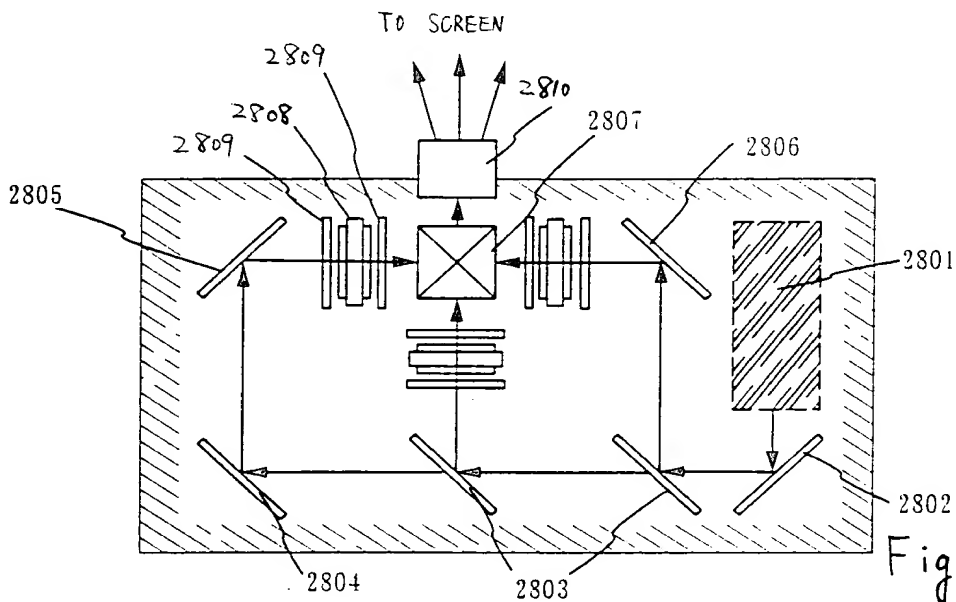
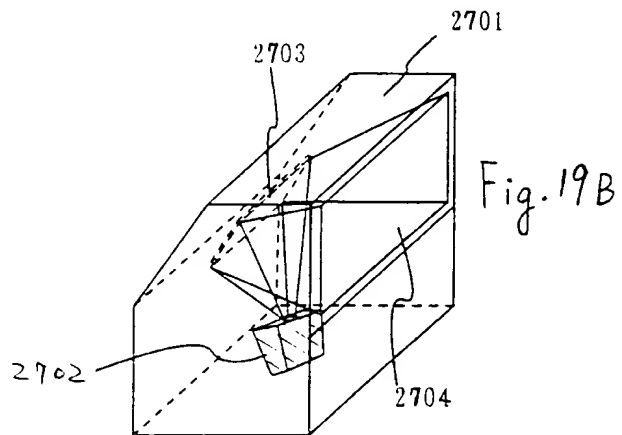
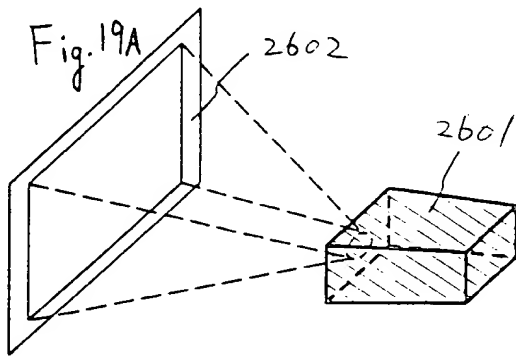


Fig. 19C PROJECTION
DEVICE
(THREE PLATE
TYPE)

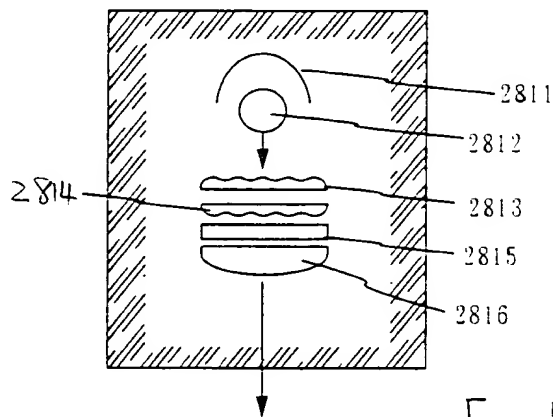


Fig. 19D LIGHT SOURCE
OPTICAL SYSTEM

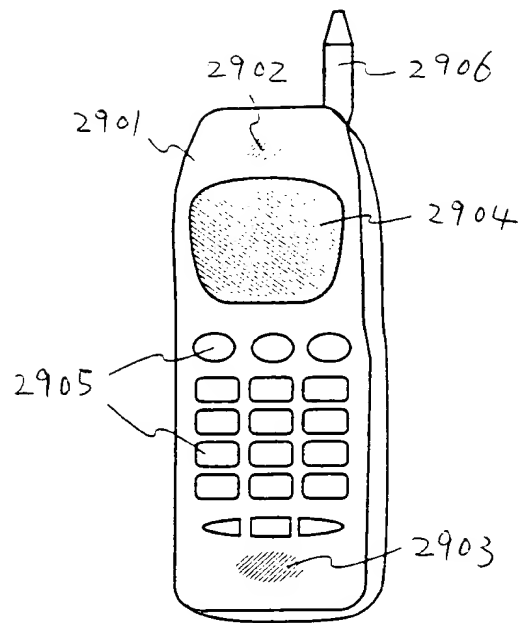


Fig. 20A

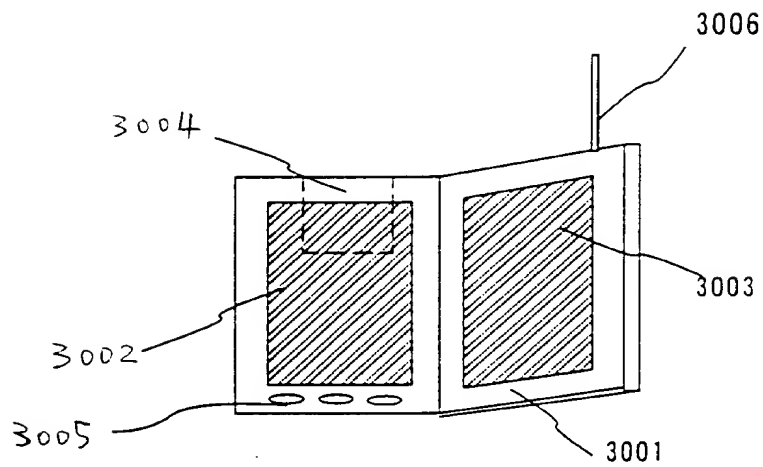


Fig. 20B

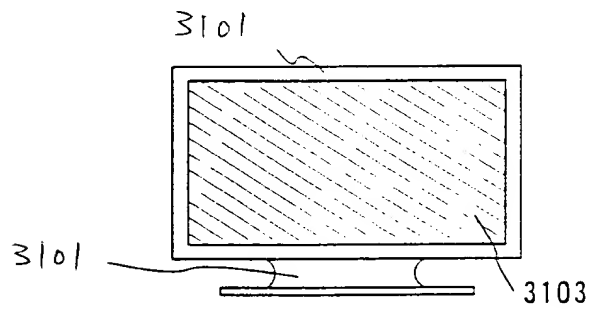


Fig. 20C

Fig. 21A

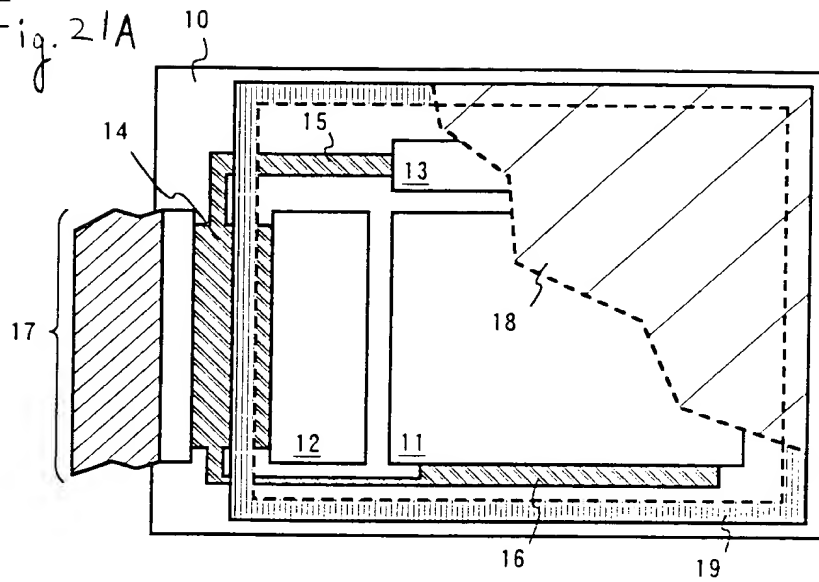


Fig. 21B

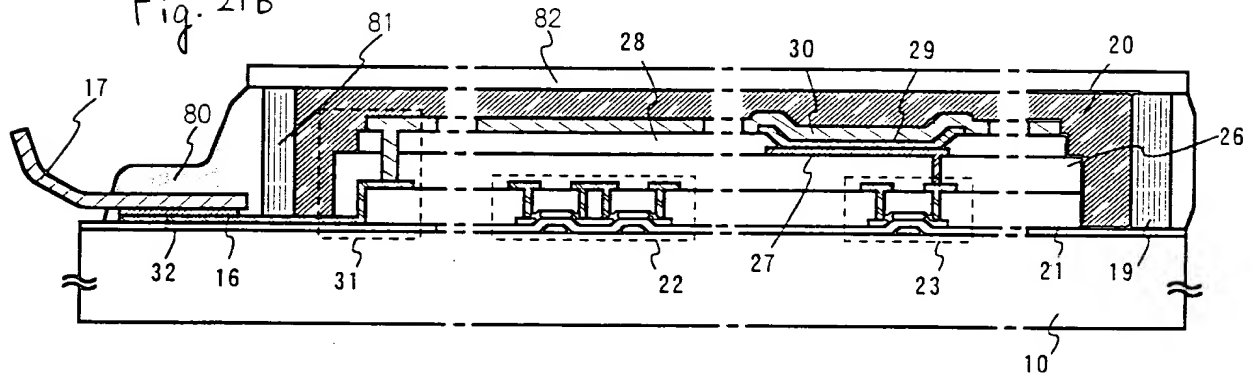


Fig. 22

